

ABSTRACT

To achieve a PLL circuit capable of operating in a broad band, let the PLL circuit be formed of two separate loops one of which is for feed-back of an output from an oscillator to this oscillator through its associative proportional control unit and the other of which is for feed-back of an output of the oscillator to the oscillator via an integral control unit. The proportional controller is for use in controlling an output frequency of the oscillator and is operable to generate a control signal based on a difference between input and output signals. The integral controller is for control of the phase of an output signal of the oscillator to thereby generate a control signal based on a phase difference between input and output signals. Further, the PLL circuit employs a current-controlled oscillator while letting the integral controller for phase synchronization consist essentially of a phase comparator and charge pump circuit plus V/I conversion circuit as well as T/I converter. And, apply a current switch circuit made up of a current switch with its control electrode forward-biased and a current switch driving complementary output voltage switch with its output connected to a low voltage-side electrode of the current switch to more than one current switch of the charge-pump circuit and/or T/I converter circuit. THE

Sub A

PCT

世界知的所有権機関
国際事務局

特許協力条約に基づいて公開された国際出願



(51) 国際特許分類 H03L 7/13, H03K 17/30, G06F 1/04, 1/301, H03M 1/80	A1	(11) 国際公開番号 WO99/00903 (43) 国際公開日 1999年1月7日(07.01.99)
--	----	--

(21) 国際出願番号 PCT/JP98/02870	栗田公三郎(KURITA, Kozaburo)[JP/JP]
(22) 国際出願日 1998年6月26日(26.06.98)	〒198-0024 東京都青梅市新町5-13-14 Tokyo, (JP)
(30) 優先権データ 特願平9/171470 特願平9/248701	(74) 代理人 弁理士 浅村 皓, 外(ASAMURA, Kiyoshi et al.) 〒100-0004 東京都千代田区大手町2丁目2番1号 新大手町ビル331 Tokyo, (JP)
(71) 出願人 (米国を除くすべての指定国について) 株式会社 日立製作所(HITACHI, LTD.)(JP/JP) 〒101-8010 東京都千代田区神田駿河台四丁目6番地 Tokyo, (JP)	(81) 指定国 JP, KR, US.
(72) 発明者 ; および (75) 発明者 / 出願人 (米国についてのみ) 加藤和男(KATO, Kazuo)[JP/JP] 〒319-1106 茨城県那珂郡東海村白方1693-6 Ibaraki, (JP) 佐瀬隆志(SASE, Takashi)[JP/JP] 〒319-1225 茨城県日立市石名坂町一丁目19-1-104 Ibaraki, (JP) 堀田多加志(HOTTA, Takashi)[JP/JP] 〒319-1224 茨城県日立市南高野町3-5-12 Ibaraki, (JP) 青木郭和(AOKI, Hirokazu)[JP/JP] 〒192-0041 東京都八王子市中野上町1-30-4 レジデンス増田401 Tokyo, (JP)	添付公開書類 国際調査報告書

(54) Title: PHASE LOCK CIRCUIT, INFORMATION PROCESSOR, AND INFORMATION PROCESSING SYSTEM

(54) 発明の名称 位相同期回路、情報処理装置及び情報処理システム

(57) Abstract

A PLL circuit operable in a wide band comprises two loops, i.e. a loop for feeding the output of an oscillator back to the oscillator through a proportional control section, and a loop for feeding the output of the oscillator back to the oscillator through an integral control section. The proportional control section controls the output frequency of the oscillator and produces a control signal from the difference between the input and output signals. The integral control section controls the phase of the output signal of the oscillator and produces a control signal from the phase difference between the input and output signals. The integral control section for locking the phase by applying a current-controlled oscillator to the PLL circuit comprises a phase comparator, charge pump circuit, a V/I conversion circuit, and a T/I converter. A current switch circuit comprising a current switch having a forward-biased control electrode and a voltage switch used for driving the complementary output current switch and having an output connected to the low voltage side electrode of the current switch is applied to the current switch for the charge pump circuit and the T/I conversion circuit.

